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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/584,728	06/01/2000	Tsutomu Yoshimura	49657-700	5073
20277 75	90 01/07/2004		EXAMINER	
MCDERMOTT WILL & EMERY			TRAN, KHANH C	
600 13TH STRI WASHINGTON	EEI, N.W. N, DC 20005-3096		ART UNIT	PAPER NUMBER
	,		2631	
			DATE MAILED: 01/07/2004	6

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)			
Office Assistant Commence	09/584,728	YOSHIMURA ET AL.			
Office Action Summary	Examiner	Art Unit			
	Khanh Tran	2631			
The MAILING DATE of this communication a Period for Reply	ppears on the cover sheet wit	h the correspondence address			
A SHORTENED STATUTORY PERIOD FOR REP THE MAILING DATE OF THIS COMMUNICATION - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication If the period for reply specified above is less than thirty (30) days, a re - If NO period for reply is specified above, the maximum statutory perio - Failure to reply within the set or extended period for reply will, by statt - Any reply received by the Office later than three months after the mail earned patent term adjustment. See 37 CFR 1.704(b). Status	I. 1.136(a). In no event, however, may a re ply within the statutory minimum of thirty d will apply and will expire SIX (6) MONT ute, cause the application to become ABA	ply be timely filed (30) days will be considered timely. "HS from the mailing date of this communication. ANDONED (35 U.S.C. § 133).			
1) Responsive to communication(s) filed on 17	October 2003.	·			
2a) This action is FINAL . 2b) ☑ Thi	is action is non-final.				
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims					
 4) Claim(s) 4-15 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) 5-13 and 15 is/are allowed. 6) Claim(s) 4 and 14 is/are rejected. 7) Claim(s) is/are objected to. Claim(s) are subject to restriction and/or election requirement. 					
Application Papers	·				
9) The specification is objected to by the Examin 10) The drawing(s) filed on is/are: a) accomplicant may not request that any objection to the	ccepted or b) objected to be drawing(s) be held in abeyand	ce. See 37 CFR 1.85(a).			
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.					
Priority under 35 U.S.C. §§ 119 and 120					
12) Acknowledgment is made of a claim for forei a) All b) Some * c) None of: 1. Certified copies of the priority docume 2. Certified copies of the priority docume 3. Copies of the certified copies of the priority docume * See the attached detailed Office action for a list 13) Acknowledgment is made of a claim for domes since a specific reference was included in the foreign language priority. a) The translation of the foreign language priority. Acknowledgment is made of a claim for domes reference was included in the first sentence of	nts have been received. nts have been received in Apiority documents have been au (PCT Rule 17.2(a)). st of the certified copies not restic priority under 35 U.S.C. § first sentence of the specifical provisional application has bestic priority under 35 U.S.C. §	pplication No received in this National Stage received. § 119(e) (to a provisional application) Ition or in an Application Data Sheet. ren received. §§ 120 and/or 121 since a specific			
Attachment(s)					
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 	5) Notice of Inf	ummary (PTO-413) Paper No(s) formal Patent Application (PTO-152)			

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DETAILED ACTION

1. The Amendment filed on 10/17/2003 has been entered. Claims 4-15 are pending in this Office action. Claims 1-3 have been cancelled. New claims 14 and 15 are added.

Response to Arguments

2. Applicant's arguments with respect to claims 4 and 14 have been considered but are most in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in the instant application in view of Kobayashi et al. U.S. Patent 5,576,643.

Regarding claim 4, admitted prior art discloses in figure 8 a conventional digital synchronous circuit including a multi-phase clock generating circuit 10 for outputting n clock signals CLK1 to CLKn, first latch circuits for taking in an input data signal according to corresponding ones of said plurality of clock signals,

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second latch circuits for taking in and holding outputs of first latch circuits. However, the prior art does not show a control circuit for outputting a control signal to the second latch circuits according to a change in the input data signal. Nevertheless, the missing features in prior art teachings have been found in Kobayashi et al. invention. According to one embodiment as shown in figure 2B, the data transfer circuit 6 outputs data D in response to an externally supplied transfer signal TR. The latch control circuit 7 generates a data latch signal DL based on an externally supplied latch control signal and on a data D supplied from the data transfer circuit 6. Kobayashi et al. invention provides a data transfer device, which precisely controls data transfer while preventing unstable data from being latched. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify admitted prior art to include a latch control circuit, as taught by Kobayashi et al., to solve the problem of indefinite state of data that the prior art encounters.

Kobayashi et al. invention, however, does not show a control circuit including a pulse generating circuit followed by a delay circuit as claimed in the instant application. Nevertheless, figure 6 shows a circuit diagram of a latch control circuit including an inverter circuit 9c for delaying the input data D a prescribed period of time until the input data D is stabilized, a pulse generating section for generating a latch control signal DL in response to the input data D. Since the inverter circuit 9c is implemented to only delay the input data D for a prescribed period of time until the input data D is stabilized, it would have been obvious to

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one of ordinary skill in the art at the time of invention to modify the latch control circuit, as taught by Kobayashi et al., so that the same delay circuit is implemented after the pulse generating circuit portion in the latch control circuit 70 because such modification won't have any impact on the operation of the latch control circuit 70.

Regarding claim 14, admitted prior art further shows, in figure 8, a clock phase determination circuit 50 and a selector 60 that perform the same functionality as claimed in the instant application.

Allowable Subject Matter

4. Claims 5-13 and 15 are allowed.

Regarding claim 5, said claim is directed to a digital synchronous circuit wherein the digital synchronous circuit has been amended to claim uniquely distinct features "wherein said control circuit includes a first pulse generating circuit for generating a first pulse signal according to a change in said input data signal" and "a third latch circuit for receiving said first pulse signal at a data input node and a clock input node" and "a level determination circuit for outputting a detection signal when potential of an output signal from said third latch circuit has crossed a reference potential" and "a second pulse generating circuit for generating a second pulse signal according to a change in potential of said detection signal and outputting said second pulse signal as said control

above underlined limitations obvious.

signal". The closest prior art, Kobayashi et al. (US Patent 5,576,643) disclosing a data transfer circuit device, either singularly or in combination, fail to anticipate or render the

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features "a pulse generating circuit for generating a pulse signal" and "a delay circuit for receiving said pulse signal to cause delay" in claim 4 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 703-305-2384. The examiner can normally be reached on Tuesday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 703-306-3034. The fax phone

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number for the organization where this application or proceeding is assigned is 703-

872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3800.

KCT

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